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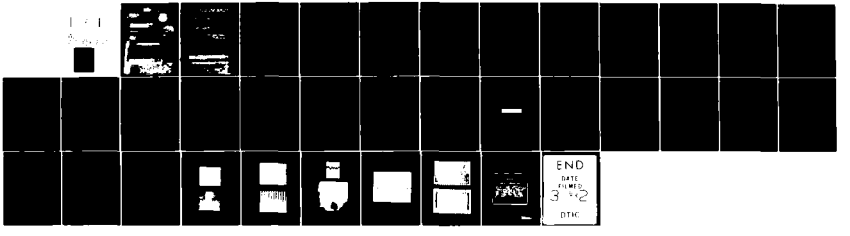

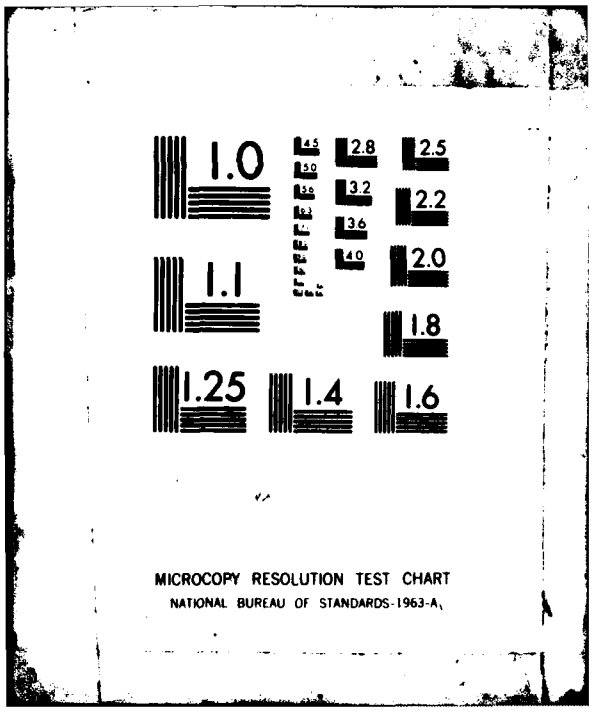
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A 256-element platinum silicide Schottky-barrier IR-CCD line sensor, developed under a prior contract, was fabricated to a matrix of processing variations and mask modification in an effort to improve the performance of the device. A new device, TC1258, resulted from the optimization study. This report details the wafer fabrication and packaging by wafer lot of all devices processed as an aid to the sponsor in evaluating the arrays.

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PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-77-C-0250. It details the chronology of certain integrated circuit devices manufactured between September 15, 1977 and June 1, 1980, in the Integrated Circuit Technology Center, D. E. O'Connor, Director. The Project Supervisor was W. F. Kosonocky. Other members of the Technical Staff who participated in this program were F. B. Shallcross; Device Processing and H. Erhardt; Device and Wafer Testing. Additional support was provided by W. S. Romito, L. M. Bijaczyk, R. Miller and G. M. Meray.

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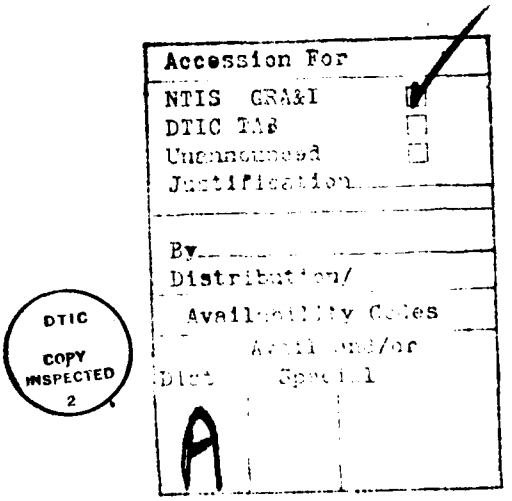

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SECTION I

INTRODUCTION

The purpose of this contract was to conduct an optimization study of a 256-element IR-CCD (Infrared Charge-Coupled Device) line sensor with platium-silicide Schottky-barrier detectors; and to provide sample quantities of this device to RADC/ET for the Infrared Fense Sensor Development Program. The mask set used in the study was that of a 256-element device developed as a second generation IR-QCD array under Air Force Contract F19628-76-C-0254.[1]

A. DESCRIPTION OF THE TC1204 ARRAY (Prior Contract Summary)

This device was designed with dual CCD-output registers to facilitate either the moving-target indicator or background subtraction mode of operation. The platinum silicide Schottky-barrier detectors with implanted N-type guard rings were integrated on-chip with double-polysilicon, buried-channel, 2-phase CCD output registers. At 77 K, the buried-channel CCD output registers had a measured charge-transfer loss of 5×10^{-5} per transfer. The Schottky-barrier detectors were designed for operation in a continuous-charge-skimming mode that resulted in a very low leakage current density measured at 1.4×10^{-9} A/cm^2 at 77 K. The quantum efficiency coefficient C_1 of the platinum silicide Schottky-barrier detectors were estimated to be 0.1, and detector-to-detector response uniformity of 8 percent maximum peak-to-peak or about 1.2 percent rms, was measured at the conclusion of the initial program.

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1. W. F. Kosonocky, D. J. Sauer, and F. V. Shallcross, "256-Element Schottky-Barrier IR-CCD Line Sensor," Final Report, Contract No. F19628-76-C-0282, September 1977.

B. SUMMARY OF OBJECTIVES

The planned objectives of the current optimization study included the fabrication of at least four (4) differently modified lots of the 256-element IR-CCD for the purpose of achieving improvements in: (a) The quantum yield of the platinum-silicide detectors; (b) The detector response uniformity; and (c) The detector area utilization.

C. PROCESSING SUMMARY (Current Program)

A total of nine (9) lots, numbered 4-12, of the TC1204 array were processed to a matrix of fabrication and design rule experiments during the study. A new mask set was then generated based on the results of the knowledge gained from the TC1204 arrays. One lot of the new arrays, TC1258, was then processed and evaluated.

SECTION II

CHRONOLOGY OF DEVICE FABRICATION (TC1204)

This section presents the description of scientific work by quarterly periods for the term of the study and includes device fabrication experiments as well as packaging and testing of continuing work conducted in the same reporting period.

A. SUMMARY OF WORK: FIRST QUARTERLY PERIOD (Sept., 1977 - Dec., 1977)

1. Processed Wafer Lots

Three wafer lots were completed of TC1204 IR-CCD line sensors. They are Wafer Lots No. 4, No. 5, and No. 6. The Wafer Lot No. 4, that was started before the reporting period, was done following our standard N+-gate double-polysilicon process. This wafer lot was split into two parts. One part of this lot with four wafers (Wafers Nos. 2, 3, 4 and 5) was processed with implanted N-type guard rings and our standard 600 Å platinum sintered for ten minutes at 650°C and annealed for twenty minutes at 430°C in forming gas. The Wafers Nos. 3 and 5 of this part of the lot No. 4 were processed with 0.9 mil-wide N-type guard rings will clearly define the width of the effective detector regions. The other two wafers of this part of lot No. 4 (Wafers Nos. 2 and 4) were processed with 0.5 mil-wide Schottky contacts which coincide with the perimeter of the N-type guard rings. The other four wafers of lot No. 4 (Wafers Nos. 1, 6, 7 and 8) were processed without the N-type guard rings for the platinum-silicide detectors. In this part of lot No. 4, Wafers Nos. 1 and 8 were formed with 2000 Å thick platinum and Wafers Nos. 6 and 7 with 1000 Å thick platinum. The suggestion of forming a thickness layer of platinum

silicide was made by S. Roosild of RADC/ET as an approach to reduce the electric field at the perimeter of the platinum-silicide detectors. A total of thirty-six operable devices were found in the Wafer Lot No. 4.

The Wafer Lot No. 5 was done with our N+-gate self-aligned process. The main purpose of this wafer lot was to obtain devices with a minimum capacitance at the floating-diffusion output-sensing mode. However, no operating devices were obtained from this wafer lot due to an excessive etching of the phosphorus-doped reflow glass by the platinum-predeposition HF dip.

The Wafer Lot No. 6 was done with our standard N+-gate process. Four wafers of this lot (Wafers A, C, D and F) were processed with platinum silicide sintered for ten minutes at 650°C and annealed for twenty minutes at 530°C in forming gas. The other four wafers of this lot (Wafers B, E, G and H) were processed with platinum silicide sintered and annealed at 320°C for eight hours in nitrogen and then for another eight hours in forming gas. A total of 45 operable 256-element IR-CCD line sensors were found in the Wafer Lot No. 6. A lower than expected device yield of this lot was also apparently due to overetching of the phosphorus-doped reflow glass by the platinum-predeposition HF dip. However, unlike in the case of the wafer Lot No. 5, this overetching was not as fatal. Steps have been taken to prevent the reoccurrence of the platinum-predeposition HF dip problem.

2. Partially Completed Wafer Lots

The Wafer Lot No. 7 is being processed to study the possibility of wide platinum-silicide detectors without N-type guard rings. This lot is being done following our P+ polysilicon gate process which up till now tends to give us the best device yield. Two of the wafers of this lot (Wafers A

and B) were processed with implanted N-type guard rings. These wafers will serve as the standard for comparison of the detector leakage current with the other remaining five wafers processed without the guard rings. The five wafers without the guard rings were split into two groups. One group (Wafers C and D) was processed with 0.2 mil P+-channel stops separating the platinum-silicide detectors. The other group of wafers (Wafers E, F and G) was processed without the P+-channel stops separating the platinum-silicide detectors. This was accomplished by a photocomposition operation using the channel stop mask in conjunction with the Schottky contact mask. This approach, relying on the operation of the Schottky-barrier detectors in the continuously charge-skimming mode, should give us the way for forming 1.0 mil-wide detectors on 1.6-mil centers without any alignment problems of the Schottky contacts with the P+-channel stops. The Wafer Lot No. 7 is scheduled for platinum silicide at the beginning of January, 1978, at which point the wafers will be divided again into two groups. One group of wafers will be completed with the 650°C platinum silicide and the other group with the 320°C platinum silicide.

The second partially completed Wafer Lot No. 8 is being processed with out self-sligned process. This lot is intended as the replacement for the Wafer Lot No. 5 to study the operation of IR-CCD line sensors with a minimum capacitance floating-diffusion output-sensing mode.

3. Program Review

A program review meeting was held at RADC/ET on October 26, 1977. Present at that meeting were B. Capone, W. Kosonocky, S. Roosild, F. Shepherd, L. Skolnik and R. Taylor. The main decision at this meeting was that additional masks will be made for the 256-element IR-CCD line sensors to obtain:

(a) A 4-mil wide output register; and

(b) 1-mil x 8-mil platinum-silicide detectors.

B. SUMMARY OF WORK: SECOND QUARTERLY PERIOD (Dec., 1977 - March, 1978)

1. Processed Wafer Lots

Three wafer lots were completed of RC1204 IR-CCD line sensors. They were Wafer Lots Nos. 7, 8 and 9. The Wafer Lots Nos. 7 and 9 were processed as an experiment to test the possibility of constructing the following two types of platinum-silicide detectors: (1) Without the N-type guard rings; and (2) Without the P+-channel stops between the detectors as well as the N-type guard rings. The channel stops between the detectors were deleted by means of multiple exposures of the Schottky contact masks used in conjunction with the exposure of the regular channel-stop mask. These two lots were also split up for two types of sintering procedures for the platinum silicide detectors. One group of wafers was sintered for ten minutes at 650°C, annealed in hydrogen for thirty minutes at 530°C, and the other group of wafers was sintered and annealed for sixteen hours at 320°C. The Schottky contacts for the above devices were 0.9-mil wide.

Wafer Lot No. 8 was made with out self-aligned process in which the n+ diffusions are self-aligned with either the polysilicon gates or the thick oxide regions. The platinum-silicide detector regions in this lot were also defined by the 0.9-mil wide Schottky contact hole mask. The effective width of the platinum-silicide detectors, however, is determined by the 0.5-mil wide openings in the n+ guard rings. Lot No. 8 was made to demonstrate the operation of the 256-element IR-CCD line sensors with a reduced capacitance of the floating diffision of the output amplifier. The full-well signal of the output register in these devices corresponds to 2.7V at the output which is about 4.5 times larger than the maximum output in the case of the devices processed by our standard, non-self aligned process. This means that the effective

capacitance of the floating diffusion of the devices made by the self-aligned process is about 0.044 pF.

As in the case of wafers from Lot Nos. 7 and 9, the wafers from Log No. 8 were also split between the devices with platinum silicide sintered and annealed at low and high temperatures.

2. Results of Measurements on Bonded Devices

Out of a total of 119 256-element IR-CCD line sensors bonded, only 43 devices were found operational after bonding. All the bonded devices were operated at room temperature as CCDs at the probe test. The rather low bonding yield is attributed to pin holes in the bonding pads formed during the probe testing. This problem will be further investigated before we will proceed with bonding any more of the TC1204 IR-CCD line sensors.

Dark current measurements were made on a number of the 256-element IR-CCD line sensors from Lots Nos. 4, 7, 8 and 9. In these tests, the devices were immersed in a liquid nitrogen; but a provision was made to keep the devices in a dry nitrogen atmosphere during the warm-up period.

Since we have lost some devices following the liquid nitrogen tests, all the available devices were not tested at low temperature. Also the results obtained on the tested device have not been completely conclusive. For example, the tests indicate that while the devices made with n-type guard rings tend to have fewer dark current spikes, we have also obtained comparable performance for devices made without guard rings--especially for operation with low reverse bias voltages on the Schottky diodes. The tested devices made without the channel stops (as well as without the n-type guard rings) in Lot No. 7 exhibited some dark current spikes for the detector diode voltage above three to four volts. However, the same type of device in Lot No. 9 gave no dark current spikes up

to the detector-diode reversed bias voltage of 9.0 volts. (It may be noted that this last device came from Wafer F which was sintered and annealed for sixteen hours at 320°C). Our present conclusion is that, by duplicating the performance of the devices in Lot No. 9, we should be able to obtain low dark current in the devices made without the guard rings and with no channel stops between the platinum-silicide detectors.

With the devices of Lot No. 8 made with the self-aligned process, we have demonstrated the possibility of decreasing the floating-diffusion output sensing capacitance by a factor of about 4.5. At liquid nitrogen temperature, the tested devices of Lot No. 8 did not show any dark current spikes at the maximum available reverse bias corresponding to V_{GIT} = +10V. These devices, however, also exhibited a very low sensitivity to infrared signal. The cause of the low IR sensitivity in Lot No. 8 has not yet been determined.

3. Additional Masks for TC1204 Devices

Five additional masks were designed and coded. With these new masks, we will be able to process the 256-element IR-CCD line sensors with a 4-mil wide output register. To increase the charge handling capacity of these arrays, the channel-stop masks were designed with correspondingly larger charge storage wells under the gates G_{2T} and G_{3T}. The new set of masks includes two channel-stop masks. The first channel-stop mask has no channel stops between the detectors. This channel-stop mask will be used in conjunction with a Schottky contact mask with 1.4 x 8.0-mil contact openings.

The second channel-stop mask was designed as part of a back-up approach to fabricate 0.8 x 8.0-mil platinum-silicide detectors with n-type guard rings. These devices will include P+-channel stops between the detectors. The processing of these back-up devices will also require the two additional

masks. They are a Schottky-contack mask with 1.0-mil x 8.0-mil contacts and a buried—channel implant mask that will also include the n-type guard rings with 0.8-mil x 8.0-mil openings defining the active areas of the detectors.

We are expecting to process the first lot of the modified devices with 4-mil wide output registers and 1.4-mil x 8.0-mil platinum silicide detectors by July 1, 1978.

C. SUMMARY OF WORK: THIRD QUARTERLY PERIOD (March, 1978 - June, 1978)

1. Additional Modified Masks for TC1204 IR-CCDs

Five additional mask levels were obtained for processing the 256-element IR-CCD line sensors with 4-mil wide output registers and wider detectors. With these new masks we will be able to fabricate the IR-CCD line sensors with 1.0-mil or 1.4-mil wide platinum-silicide detectors without the n-type guard rings and without p+—channel stops between the detectors. As a backup we will also be able to fabricate the IR-CCD line sensors with 0.8-mil wide detectors that will include the n-type guard rings and the p+ channel stops between the detectors.

2. Wafer Processing

Using the new modified mask set, we are processing the Wafer Lot No. 10 of TC1204 IR-CCD line sensors. In this wafer lot, the platinum-silicide detectors will have no guard rings and no channel stops. The wafer lot was split into two groups of wafers. One group is fabricated with 1.0-mil wide detectors and the other group with 1.4-mil wide detectors. The group with 1.0-mil wide detectors will be metallized with aluminum covering the platinum-silicide detectors and the group with the 1.4-mil detectors will be fabricated with the metallization option in which the aluminum does not cover the platinum-

silicide detectors. Lot No. 10 will be fabricated with the IR detectors formed from 600 Å thick platinum that is subsequently sintered for thirty minutes at 650°C and annealed in forming gas for twenty minutes at 530°C.

D. SUMMARY OF WORK: FOURTH QUARTERLY PERIOD (June, 1978 - Sept., 1978)

1. Wafer Lot No. 10

Wafer Lot No. 10 was fabricated with p+ polysilicon gates. The detector in this wafer lot has no guard rings and channel stops. The platinum thickness was 600 Å and the platinum silicide was sintered at 650°C for thirty minutes in forming gas and then annealed in forming gas for twenty minutes at 530°C. Wafers A, B and C in Lot No. 10; i.e.:

TC1204-10-A

TC1204-10-B

TC1204-10-C

were fabricated with 1.4-mil wide Schottky contacts. Also a metal option was used which left the detectors not covered by the aluminum.

Wafers D, E, F and G of Wafer Lot No. 10; i.e.:

TC1204-10-D

TC1204-10-E

TC1204-10-F

TC1204-10-G

were fabricated with 1.0-mil wide Schottky contacts with aluminum covering the detectors.

The first probe testing of the wafers in Lot No. 10 gave no operable devices. Out investigation revleaed that the yield loss was due to metal shorts at the edges of the second-level polysilicon. To correct the problem

we have reworked all of the wafers in Lot No. 10. This involved stripping the aluminum, depositing a 3000 Å thick layer of SiO_2, opening the contacts in the CCD area (not the Schottky contacts), and redepositing and redefining the aluminum. The reworked wafers yielded 29 working devices at the second probe testing of Lot No. 10.

The bonding of three of these devices from Lot No. 10 was completed. An additional 21 devices are being bonded.

It should be noted that the finished devices in Lot No. 10 have a 3000 Å thick layer of deposited SiO_2 over the platinum silicide detectors.

2. Wafer Lot No. 11

Wafer Lot No. 11 was also processed with P+ polysilicon gates. The detectors in this lot were formed with implanted n-type guard rings and separated by p+-channel stops. The Schottky contacts in this lot are 1.0-mil wide; but the effective size of the detectors is 0.8 x 8.0 mil, defined by the implanted guard rings.

Wafers A, B and F of this lot were fabricated with out standard (∿1000 Å thick) thermal oxide insulating the second-level polysilicon. In an attempt to improve the yield, Wafers C, D and E of this lot were fabricated with the second-level polysilicon insulation in the form of the standard thermal oxide plus a deposited 3000 Å thick SiO_2.

The platinum silicide on Wafers A, B, D and E was formed from a nominal 600 Å thick platinum. However, a thin, 100 Å to 120 Å, platinum was E-beam evaporated on Wafers C and F. All wafers were sintered at 320°C for eight hours in nitrogen and eight hours in forming gas. Furthermore, in Wafers C and F, the thin platinum silicide detectors were insulated with 3000 Å thick deposited SiO_2. Finally, all wafers in Lot No. 11 were processed with aluminum covering the platinum silicide detectors.

At the initial probe testing of Lot No. 11, we have obtained the following yield of operable devices:

WAFER NO.	NO. OF OPERABLE DEVICES
TC1204-11-A	3
TC1204-11-B	4
TC1204-11-C	12
TC1204-11-D	4
TC1204-11-G	5
TC1204-11-F	9

Wafers C, G and F were diced and twenty-five devices were bonded. Wafers A and D were reworked by stripping the aluminum depositing a 3000 Å thick SiO_2 insulating layer, opening the CCD contacts, and redepositing and redefining the aluminum. Note, in Lot No. 11 Wafers A, C, D and F have the 3000 Å SiO_2 layer over the platinum silicide detectors. In Wafer A, the probe yield of operable devices increased from 3 to 10 due to the reworking, and in Wafer D from 4 to 6.

3. Wafer Lot No. 12

Wafer Lot No. 12 is similar to Wafer Lot No. 10 except it has been fabricated with n+ polysilicon gates and the associated reflow glass process. The processing of Lot No. 12 was stopped prior to the Schottky contact step. This will allow us to choose the procedure for the formation of the platinum silicide detectors after we receive from RADC/ESE the performance results on the devices from Wafer Lot Nos. 10 and 11.

4. Package Modification for TC1204 Devices

In order to simplify the bonding of the TC1204 devices, we have developed a procedure for raising by machine pressing the package platform

on which the chip is bonded. The modified packages are much easier to bond as they do not require refocusing of the microscope at each bonding step.

E. SUMMARY OF WORK: FIFTH QUARTERLY PERIOD (Sept., 1978 - Dec., 1978)

1. Wafer Lots Nos. 10 and 11

We have bonded twenty-two 256-element IR-CCD line sensors from Wafer Lot No. 10. Thirteen of these line sensors were delivered to RADC/ESE. We have also bonded forty 256-element IR-CCD line sensors from Lot No. 11. Twenty-seven of the IR-CCD line sensors from Lot No. 11 were delivered to RADC/ESE.

2. Wafer Lot No. 12

As was reported in Quarterly Progress Report No. 4, the processing of Wafer Lot No. 12 was stopped prior to the Schottky contact step. The processing of this lot will be resumed with a new set of processing masks.

The low yield of operable devices in Lots Nos. 10 and 11 has been attributed to poor quality of masks. Therefore, to improve yield in wafer Lot No. 12, we have ordered a new set of masks for six processing levels. The following are the reordered new mask levels:

Mask No. 7 - Standard contact holes (not including the Schottky contacts)

Mask No. 9 - 0.5-mil wide Schottky contacts

Mask No. 21 - 1.0-mil wide Schottky contacts

Mask No. 22 - 1.4-mil wide Schottky contacts

Mask No. 10 - Metal mask with aluminum over the Schottky diodes

Mask No. 11 - Metal mask without aluminum over the Schottky diodes

Wafer Lot No. 12 is fabricated with n+ polysilicon gates and the associated reflow glass process. The 1.4-mil wide platinum silicide detectors in this lot will have no guard rings and no channel stops. In agreement

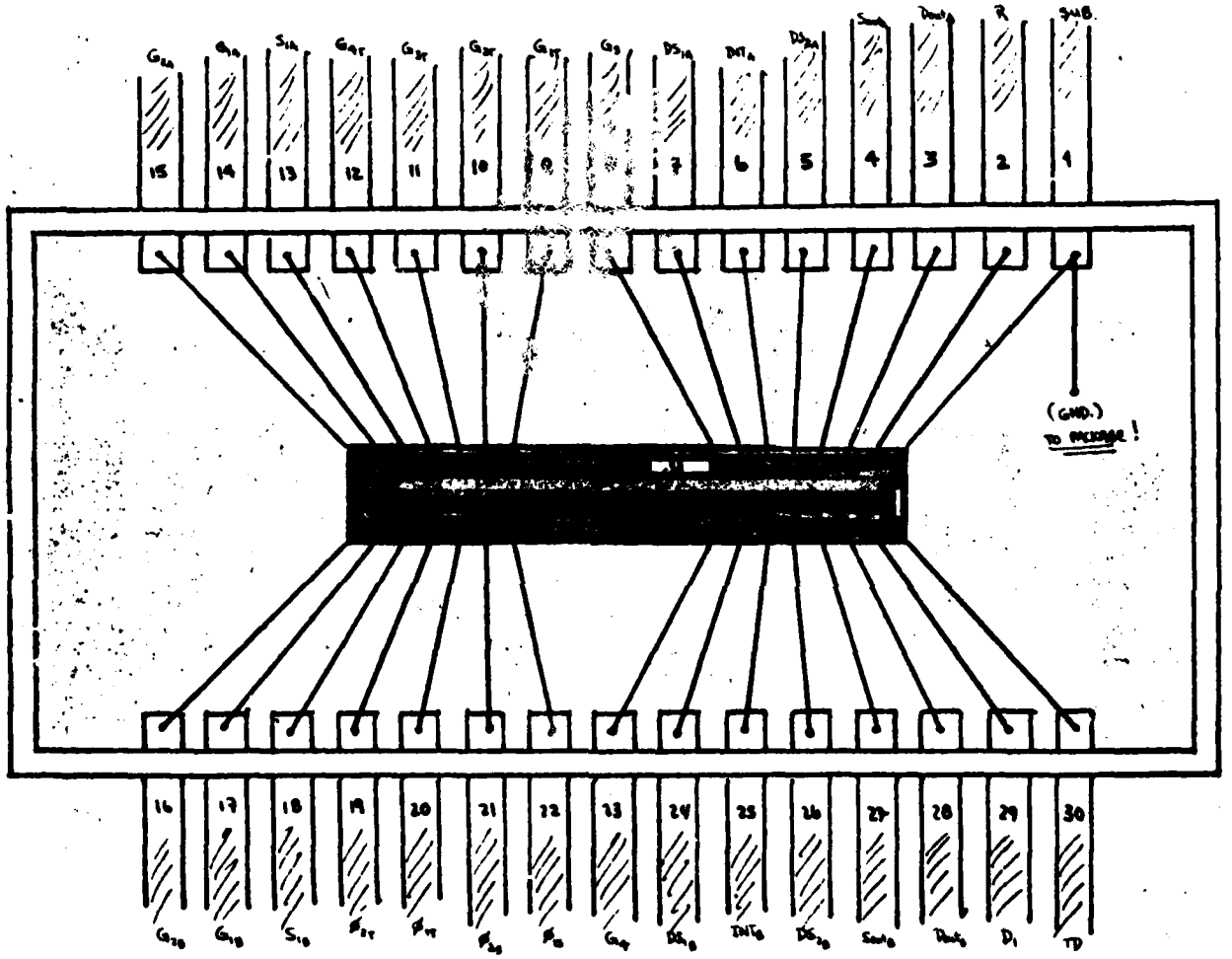


Figure 1. TC1258 bonding schematic (256 x 1 line array).

with our discussion at RADC/ESE, this wafer lot will be split into the following three groups of wafers.

3. Wafer Group A

In this group of two wafers, the detector will be formed from 100 Å thick platinum sintered for ten minutes at 650°C in forming gas. No HF will be used before deposition of aluminum. For this group, we will use the metallization mask with no aluminum over the detectors. After the definition of aluminum, the wafers will be alloyed for fifteen minutes at 450°C in forming gas.

4. Wafer Group B

In this group of two wafers, the detectors will also be formed from 100 Å platinum but sintered at 320°C for eight hours in nitrogen and eight hours in forming gas. The platinum silicide detectors will be covered with a 2000 to 3000 Å thick layer of deposited SiO_2. For definition of aluminum, we will use the mask option which forms 1.2-mil wide aluminum electrodes over the platinum-silicide detectors.

5. Wafer Group C

The wafers in this group will be processed with the platinum silicide detectors formed from a 600 Å thick platinum sintered also at 320°C for sixteen hours. We will use our standard HF dip before the deposition of aluminum. This group of wafers will represent the devices made following our standard processing procedure for IR-CCDs.

F. SUMMARY OF WORK: SIXTH QUARTERLY PERIOD (Dec., 1978 - March, 1979)

New masks were obtained for: (1) Contact holes; (2) Schottky contacts; (3) Metal with aluminum over the Schottky diodes; and (4) Metal without aluminum over the Schottky diodes. Using the above masks, we have completed Wafer Lot No. 12. Wafer Lot No. 12 was processed with n+ polysilicon gates and phosphorus-doped reflow glass. The IR-CCD line sensors in this lot have 1.4-mil wide Schottky detectors without guard rings and channel stops between the detectors. The platinum silicide detectors in this lot were processed according to the schedule described in the last Quarterly Progress Report as follows:

The detectors in Wafers B and H were formed from 100 Å thick platinum silicide and sintered for ten minutes in forming gas at 650°C. These two wafers originally had aqua regia strip and no HF dip prior to metallization. The tests of these wafers after metallization indicated poor contacts to the n+ diffusions. Assuming the the metallization was suspect on these two wafers, the aluminum was stripped, the wafers were recleaned in the aqua regia, and the aluminum was redeposited and redefined. After this procedure, the contacts were found to be still marginal. Therefore, the metallization on these two wafers was stripped for the second time and reworked. This time, however, these wafers were given H_2SO_4:HNO_3 clean followed by a 50:1 HF dip before redeposition of the aluminum. The other five wafers on which we have used our regular cleaning procedure, including the HF dip, appeared to have good metal contact and are ready for probe testing. The detectors on Wafers C and D were also formed using 100 Å thick platinum. These wafers, however, were annealed at 320°C for eight hours in forming gas and eight hours in nitrogen. Then these wafers were subjected to an aqua regia strip, a 2500 Å thick layer of SiO_2 was deposited on the

detectors, contacts were reopened to the n+ diffusions and the polysilicon gates, and the wafers were cleaned in H_2SO_4:HNO_3 solution and had a 50:1 HF dip before deposition of aluminum. The metallization on these wafers was defined with aluminum electrodes over the platinum silicide detectors.

The detectors on Wafers E, F, and G were formed from a 600 Å thick platinum sintered at 320°C for sixteen hours. Then, after the aqua regia strip, H_2SO_4:HNO_3 clean and 50:1 HF dip, the aluminum was deposited and defined. The metallization on these three wafers was defined with aluminum electrodes over the platinum silicide.

G. SUMMARY OF WORK: SEVENTH QUARTERLY PERIOD (March, 1979 - June, 1979)

1. New Packages for TC1204 Devices

We have received 200 new packages, Isotronics IP-1055-2, for the 256-element IR-CCD line sensors, TC1204. We are expecting that the new packages will alleviate the problems that we have experienced in the TC1204 devices in the old packages, IP-1065-4. Thirty-one (31) of the IR-CCD line sensors from Lot No. 12 are being bonded in the new packages.

2. Wafer Lot No. 12

Wafers C, D and F of Lot No. 12 were reworked after probe testing. In the case of Wafers C and D, we have reopened the contacts to the n+ diffusions and polysilicon gates before redepositing and redefining of the aluminum. In the case of Wafer F, which orginally showed many shorts, we have deposited a 3000 Å thick layer of SiO_2 over the device including the Schottky diodes before opening the contact holes and redepositing and redefining of the aluminum. As we have mentioned in the last Quarterly Progress Report, Wafers B and H were reworked during the original processing.

Therefore, in Wafer Lot No. 12, only Wafers E and G were not reworked; i.e., they had the aluminum deposited and defined only once.

In Wafers B, E, G and H, we have found twenty-four 256-element IR-CCD line sensors that operated at room temperature at the probe testing. These devices were bonded in the old packages (Isotronics ID-1065-4). In the case of the reworked Wafers C, D and F, we have found a total of thirty-one operating at the probe test. These thirty-one IR-CCD line sensors are being bonded in the new packages (IP-1055-2).

The status of the devices from Wafer Lot No. 12 is summarized in Table No. 1. It should be noted that this lot was processed with n+ doped polysilicon gates and our phosphorous-silicate reflow glass. All platinum-silicide detectors are 1.4-mil wide and have no n-type guard rings and no p+-channel stops between the detectors. The wafers in this lot were divided into the following three groups:

(1) Wafers B and H with 100 Å platinum sintered at 650°C for ten minutes. The devices in this group have no deposited oxide and no aluminum electrodes over the platinum silicide detectors.

(2) Wafers C and D with 100 Å platinum sintered at 320°C for sixteen hours. The devices in this group have about 2500 Å thick deposited SiO_2 and aluminum electrodes over the platinum silicide detectors.

(3) Wafers E, F and G have 600 Å platinum sintered at 320°C for sixteen hours and have aluminum electrodes over the detectors. Wafers E and G were not reworked and have no deposited SiO_2 over the platinum silicide detectors. Wafer F was reworked and it has about 3000 Å thick deposited SiO_2 insulating the platinum silicide detectors from the aluminum electrodes.

TABLE I. STATUS OF 256-ELEMENT IR-CCD LINE SENSORS IN LOT NO. 12

Wafers	Thickness of Platinum	Temperature and Time of sintering Platinum	Thickness of dep. SiO_2 over Detectors	Aluminum Over Pt-Si Detectors	Reworked	Number of Operating Devices of Probe Test	Remarks
B	100Å	650°C 10 min.	0	No	Yes	6	
C	100Å	320°C 16 h	2500Å	Yes	Yes	14	
D	100Å	320°C 16 h	2500Å	Yes	Yes	12	
E	600Å	320°C 16 h	0	Yes	No	4	
F	600Å	320°C 16 h	3000Å	Yes	Yes	5	
G	600Å	320°C 16 h	0	Yes	No	5	
H	100Å	600Å 10 min.	0	No	No	9	

H. SUMMARY OF WORK: EIGHTH QUARTERLY PERIOD (June, 1979 - Sept., 1979)

Layout was done and the coding is expected to be completed by October 5, 1979 of the modified 256-element IR-CCD line sensor, TC1258. The TC1258 array has the following features:

a. The chip size is 438 x 71 mils. The test chip area of the TC1204 array was removed.

b. The sample-and-hold transistor of the TC1204 array was removed.

c. The output A register has a 4-mil (100 μm) wide channel.

d. The aluminum lines were modified to have a minimum width of 15 μm.

e. The masks for the TC1258 array were designed for the non-self aligned NMOS process with p+ or n+ polysilicon gates.

f. The mask set option includes provisions for processing 0.8-mil wide Schottky detectors with implanted guard rings and p+ channels as well as 1.4-mil wide Schottky detectors without p+-channel stops.

g. The 0.8-mil wide detectors can be fabricated with and without aluminum electrodes covering the detectors.

h. The aluminum electrodes can be either directly connected to the platinum silicide detectors or can be insulated from the platinum silicide detectors by a layer of deposited SiO_2.

i. Two mask options are available for the n+ diffusions. With one of the masks, the n+ diffusions extend to the platinum silicide detectors. With the other mask, the n+ diffusions connect the detectors with transfer gate G_{1T} only either via the aluminum electrode or via the n-type guard ring.

j. The 1.4-mil wide detectors can be fabricated only without aluminum electrodes over the detectors.

k. The following masks are included for processing the TC1258 array on three-inch silicon wafers:

(1) n+ diffusion I (short)

(2) n+ diffusion II (long)

(3) p+-channel stop I for 0.8-mil wide detectors

(4) p+-channel stop II for 1.4-mil wide detectors

(5) BCCD implant I with guards for the 0.8-mil wide detectors.

(6) BCCD implant II for 1.4-mil wide detectors.

(7) First-level polysilicon gates

(8) Second-level polysilicon gates

(9) Contact holes

(10) Contact holes plus 1.0-mil wide Schottky contacts

(11) Contact holes plus 1.4-mil wide Schottky contacts

(12) Contact holes plus a Schottky contact block (exposing the whole detector area)

(13) Aluminum

(14) Pad openings

One lot of these arrays was successfully processed to the above design rules. Processing is summarized in Table II. The devices were packaged and forwarded to RADC. Figure 1 includes a chip photograph and bonding diagram for the device.

I. VISUAL SUMMARY OF RESULTS OF DESCRIBED WORK

Figures 2 through 9 show the results of the work on this program.

TABLE II

256 Element IR-CCD Line Sensors, TC 1258, Lot No. 1

Wafer	Sinter 320°C 16 Hrs	Thickness of Dep. Pt (Å)	N+ Diffusion		Dep. SiO_2 over PtSi (Å)	Remarks
			Long	Short		
A	Yes	600	x		Ø	
B	Yes	<100	x		3000	
C	Yes	<100	x		5000	
E	Yes	-	x		-	
F	Yes	<100		x	5000	
G	Yes	-		x	-	
H	Yes	-		x	-	
I	Yes	600		x	0	
J	Yes	600		x	0	
K	Yes	600		x	0	

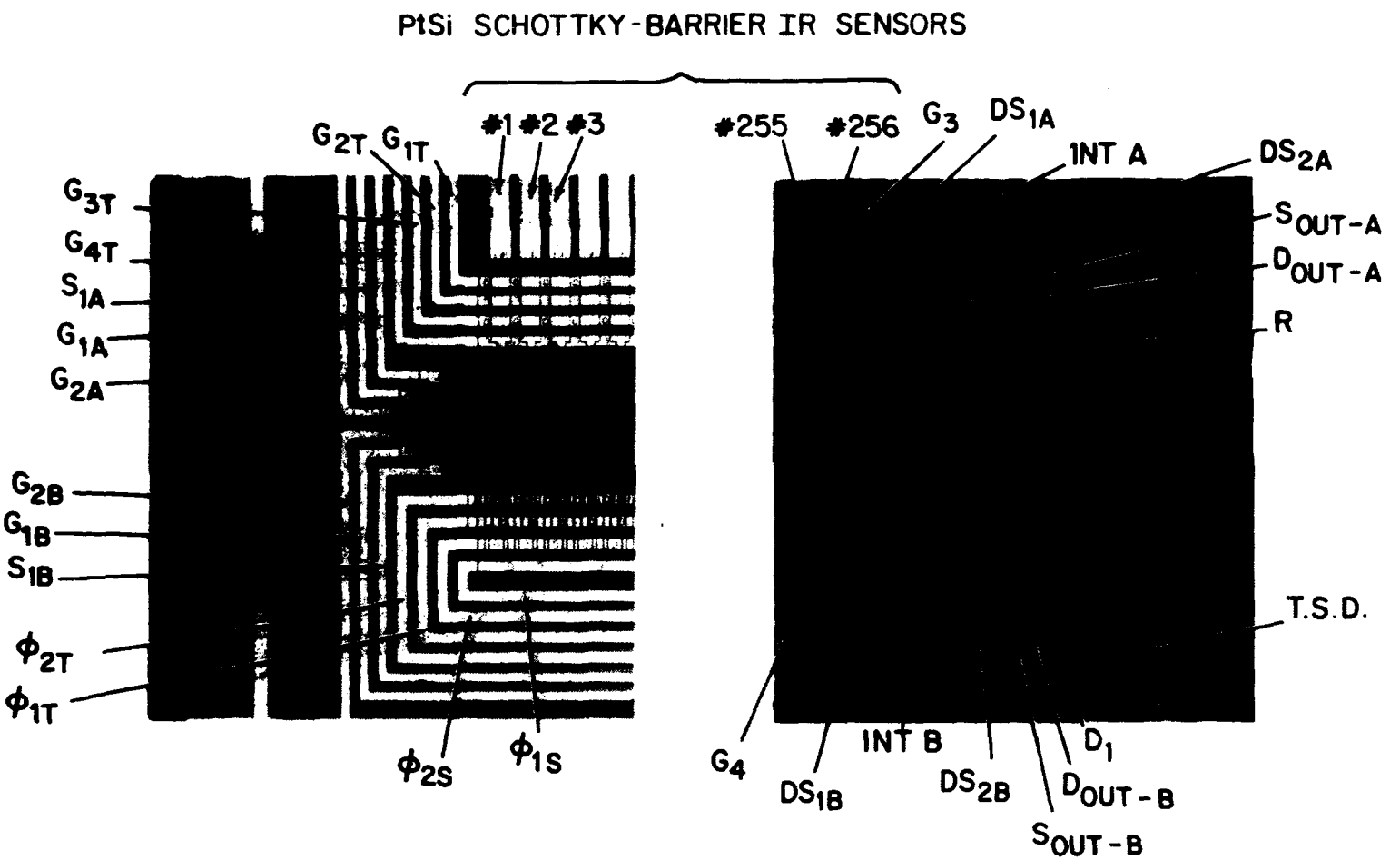


Figure 2. Photomicrograph of the input and output sections of the 256-element IR-CCD.

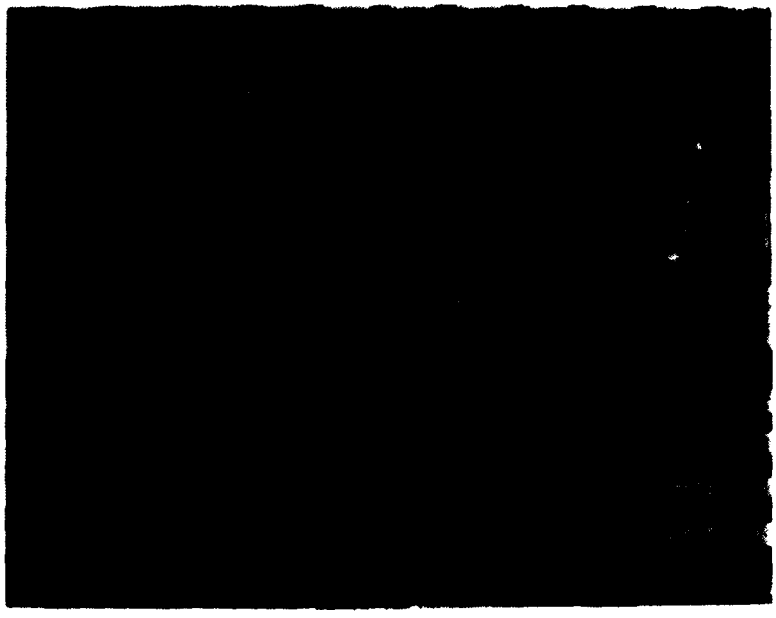


Figure 3. Photomicrograph of platinum silicide Schottky-barrier detectors with no guard ring.

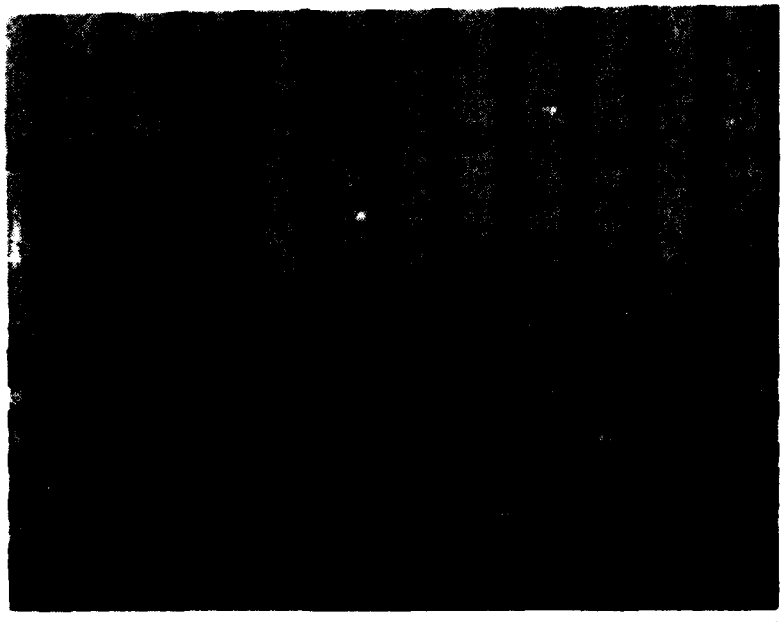


Figure 4. Photomicrograph of platinum silicide Schottky-barrier detectors with guard rings.

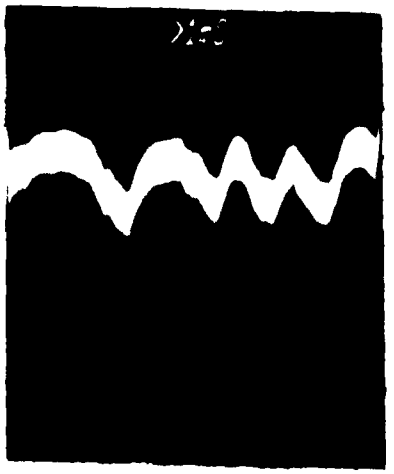


Figure 5. Thermal imagery signal of human fingers in a 300 K background.

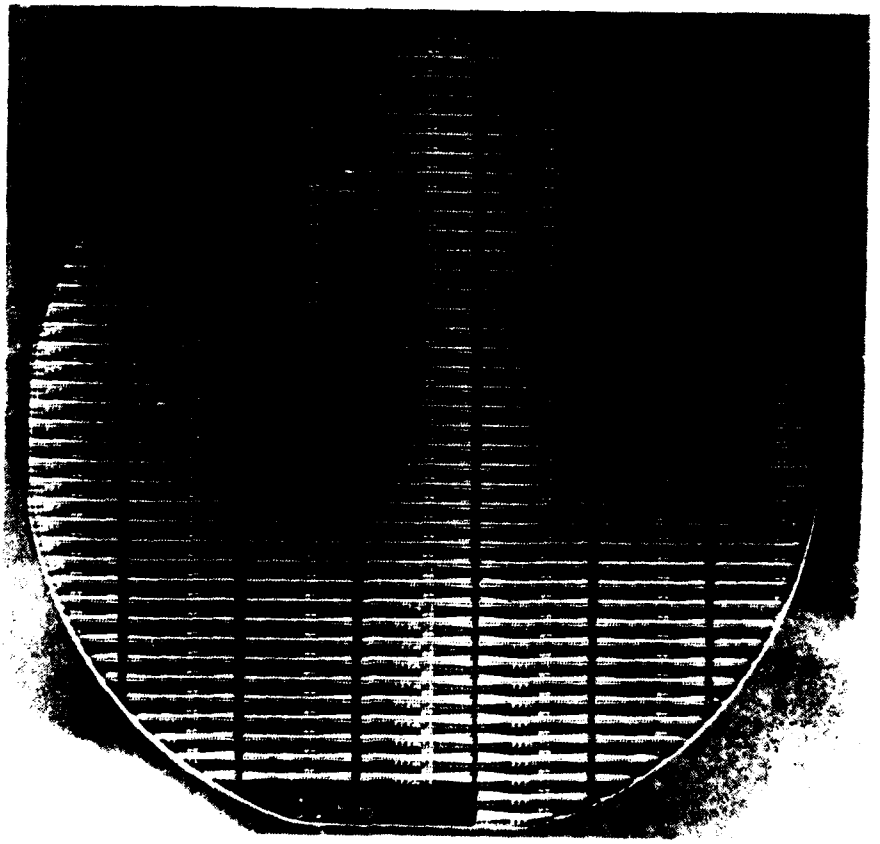


Figure 6. Three-inch wafer of TC1258 devices.

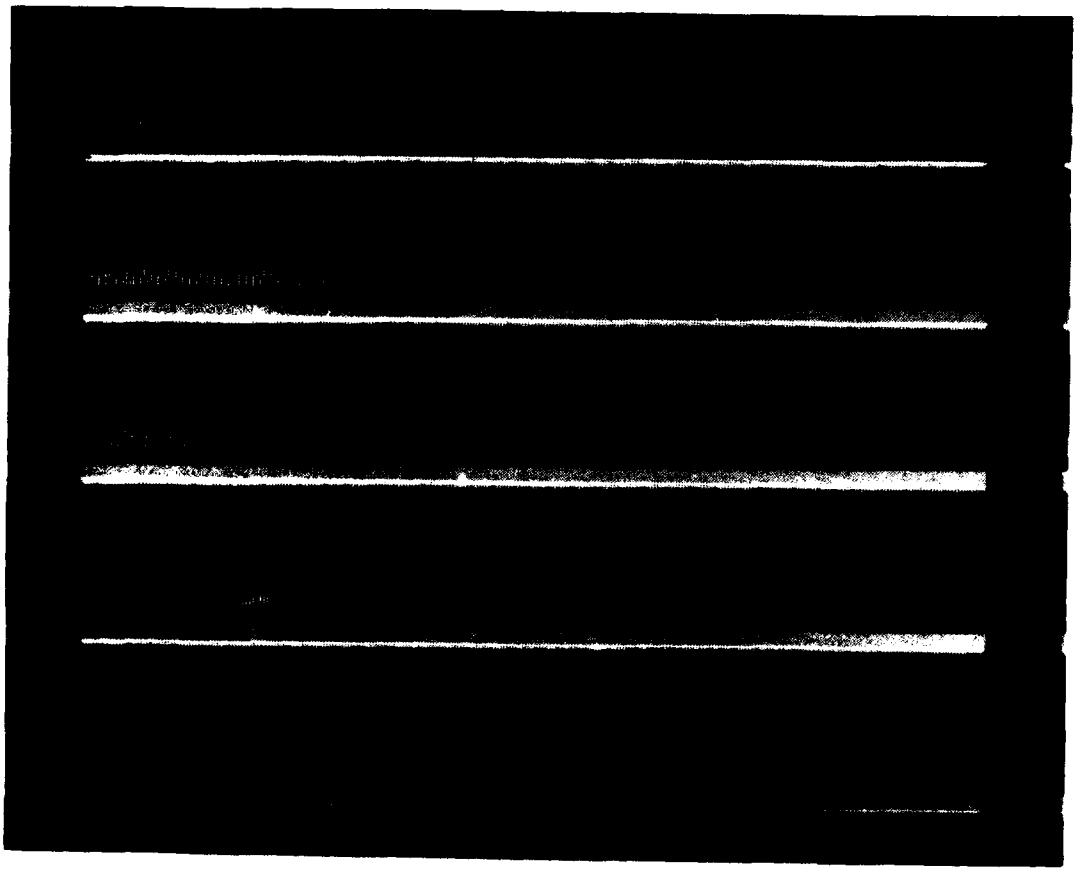


Figure 7. Wafer section with TC1258 devices.

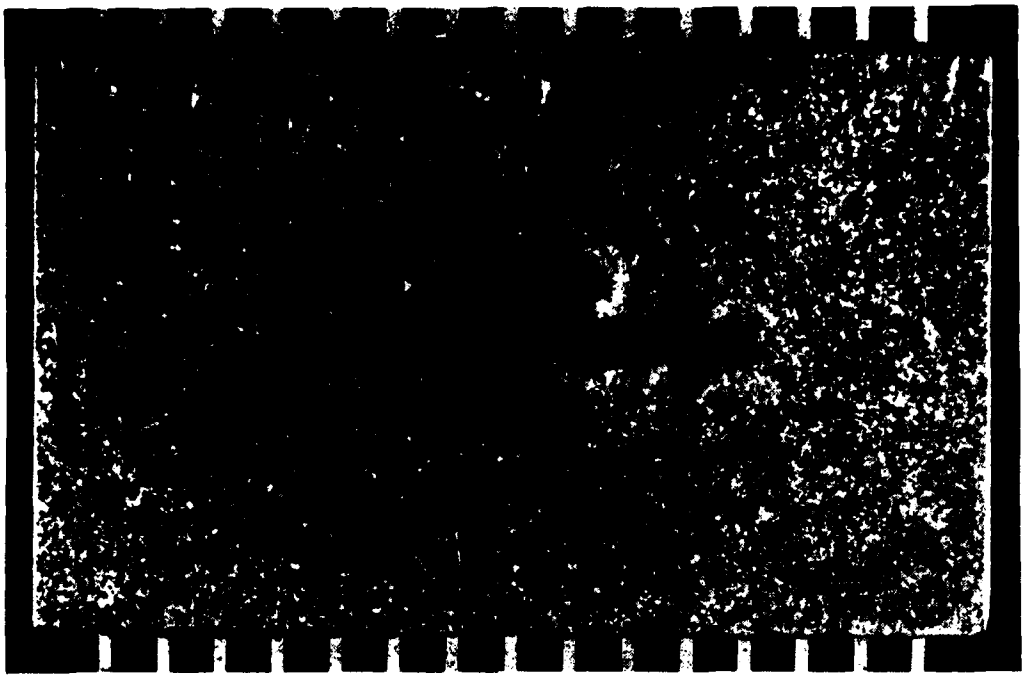


Figure 8. TC1258 package.

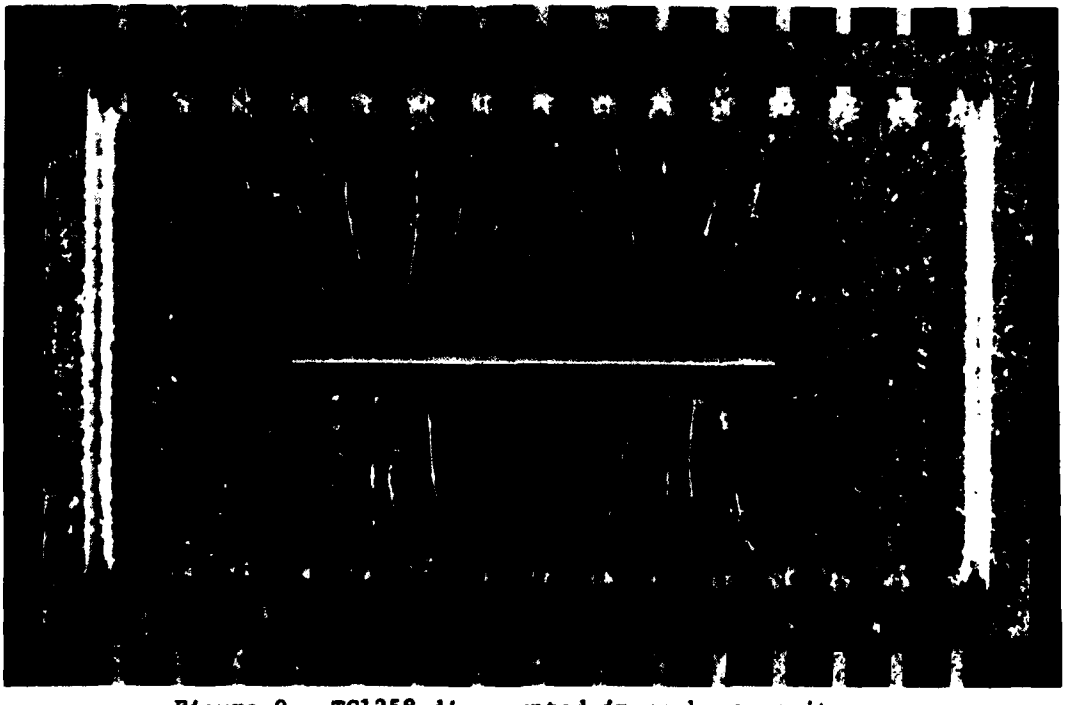
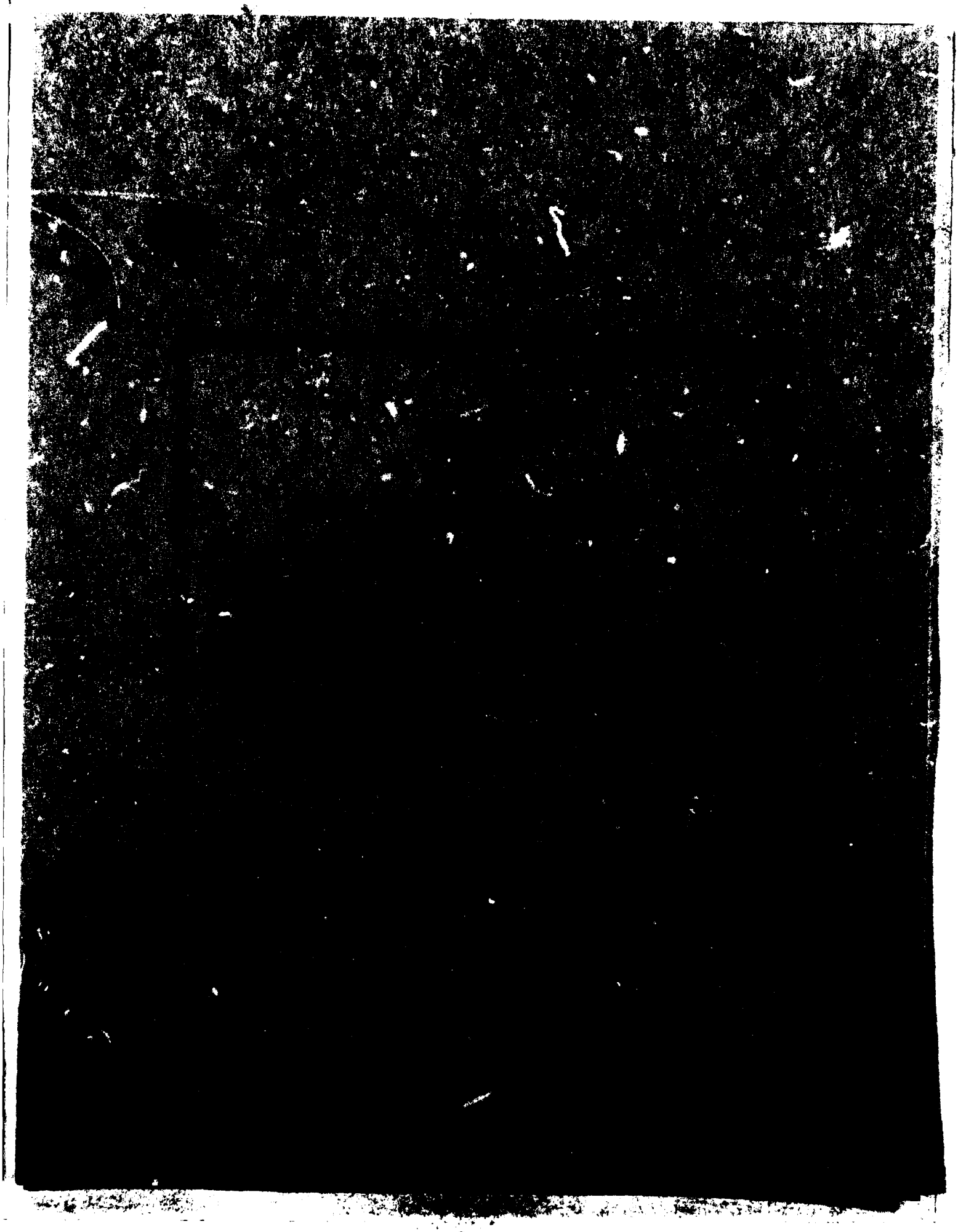


Figure 9. TC1258 die mounted in package cavity.



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